Coupled Dual LC Tanks based ILFD with Low Injection Power and Compact Size

presented by

Mahalingam Nagarajan
Research Associate
School of EEE, Nanyang Technological University, Singapore

02-10-2014
Outline

- Motivation
- Background and Fundamentals
  - Operating principle, performance metrics of ILFD
  - Different ILFD topologies
- Proposed ILFD
  - Design challenges in ILFD design
  - Proposed ILFD
  - Results and Discussion
- Conclusion and Future work
Motivation

- Unlicensed band around 60 GHz
- Large channel bandwidth
- Giga-bits-per-second applications

Motivation - High Frequency Divider

- Important Specifications
  - Locking Range
  - Power consumption
  - Phase noise
  - Output power and efficiency

- Design Challenges
  - High frequency of operation
  - Wide locking range with low injected power levels
  - High output power to drive subsequent blocks with low power consumption
Static Frequency Divider

- Popular topology based on Ring oscillator.
  \[ f_{\text{max}} \leq \frac{1}{2\pi \cdot R_L C_L} \]

- Oscillation condition: \[ g_{ML} \cdot R_L \geq 1 \]

- Advantages
  - Wide locking range
  - Small layout area

- Drawbacks
  - High power consumption
  - Poor phase noise

---

Injection Locked Frequency Divider

- **Popular topologies**
  - Ring Oscillator based ILFD
  - LC based ILFD

- **Advantages**
  - High frequency of operation
  - Low power consumption
  - High output power & Low phase noise

- **Drawbacks**
  - Narrow locking range
  - Large layout area

---

Injection Locked Frequency Divider
Design Challenge

- Locking Range of ILFD

\[
\frac{\Delta \omega}{\omega_o} = \frac{I_{inj}}{2Q \times I_{osc}}
\]

- Important Parameters
  - Injection power or efficiency \(I_{inj}\)
  - Quality factor of tank circuit
  - ILFD core current \(I_{osc}\)

- How to increase the locking range at low injected power level?
  - either quality factor of the tank circuit or ILFD core current has to decrease.

- Drawbacks?
  - Yes, high power consumption, low output power, poor phase noise
Injection Locked Frequency Divider based on Coupled Dual LC tanks

- Cross-coupled oscillator topology
- Coupled dual LC tank
- Differential injection transistor topology
- PMOS current source to reduce noise

Features
- Simple topology
- Fully differential operation
- No additional layout area
Analysis of Coupled Dual LC tanks

\[ R_s = R_1 + \frac{\omega^2 M^2 R_2}{[\omega L_2 - (\omega C_v)^{-1}]^2} \quad \text{and} \quad L_s = L_1 + \frac{\omega^2 M^2 C_v}{1 - \omega^2 L_2 C_v} \]

\[ Q = \frac{R_p \parallel R_{\text{inj}}}{\omega L_p} \]

\[ I_{\text{inj}} = g_{m,\text{inj}} v_{gs,\text{inj}} \approx g_{m,\text{inj}} V_{\text{inj}}(t) \]

\[ I_{\text{osc}} = g_{m,\text{osc}} v_o \approx g_{m,\text{osc}} \frac{I_{dc} R_{\text{inj}}}{2} \]

\[ \frac{\Delta \omega}{\omega_o} = \frac{g_{m,\text{inj}} V_i \omega L_p}{g_{m,\text{osc}} I_{dc} R_{\text{inj}}^2} \]

ILFD
Die microphotograph

- Tower Jazz 0.18 µm SiGe BiCMOS process
- $F_{\text{center}} = 12$ GHz
- $P_{\text{DC}} = 4.8$ mW with 1.8V
- Core: $0.22 \times 0.29$ mm$^2$
- Dual coupled coils:
  - Top Metal thickness: 2.81 µm
  - Area: $123 \times 123$ µm$^2$
ILFD Results
Locking Range

- Locking Range: 21.41 GHz – 25.18 GHz (16%) @ -16 dBm input
- Output Power: -2.5 dBm to -3.2 dBm
ILFD Results
Phase Noise

- Free-run: -98 dBc/Hz @ 1 MHz offset from 12.5 GHz
- Locked Phase noise: 6 dB difference with 25 GHz input
### ILFD Results

#### Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th>Ref</th>
<th>This Work</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[5]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>F&lt;sub&gt;CENTER&lt;/sub&gt; (GHz)</strong></td>
<td></td>
<td>24</td>
<td>23</td>
<td>23</td>
<td>28</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td><strong>LR (%) @</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin = -10 dBm</td>
<td></td>
<td>17.16</td>
<td>-</td>
<td>15.7</td>
<td>10.88</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Pin = -5 dBm</td>
<td></td>
<td>18.49</td>
<td>10.62</td>
<td>17.8</td>
<td>13.55</td>
<td>7.06</td>
<td>12</td>
</tr>
<tr>
<td>Pin = 0 dBm</td>
<td></td>
<td>25.07</td>
<td>11.76</td>
<td>23.7</td>
<td>21.47</td>
<td>13.08</td>
<td>16</td>
</tr>
<tr>
<td><strong>P&lt;sub&gt;DC&lt;/sub&gt; (mW)</strong></td>
<td></td>
<td>4.8</td>
<td>4.32</td>
<td>1.5</td>
<td>1.8</td>
<td>1.51</td>
<td>6.4</td>
</tr>
<tr>
<td><strong>PN (dBc/Hz)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>@ 10 kHz</td>
<td></td>
<td>-116</td>
<td>-110</td>
<td>-110</td>
<td>-105</td>
<td>-108</td>
<td>-108</td>
</tr>
<tr>
<td>@ 1 MHz</td>
<td></td>
<td>-127</td>
<td>-</td>
<td>-131</td>
<td>-124</td>
<td>-123</td>
<td>-126</td>
</tr>
<tr>
<td><strong>P&lt;sub&gt;OUT&lt;/sub&gt; / P&lt;sub&gt;DC&lt;/sub&gt; (%)</strong></td>
<td></td>
<td>18.56</td>
<td>-</td>
<td>5.29</td>
<td>2.21</td>
<td>10.5</td>
<td>11.06</td>
</tr>
<tr>
<td><strong>FOM (%/mW&lt;sup&gt;2&lt;/sup&gt;)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin = -10 dBm</td>
<td></td>
<td>6.63</td>
<td>-</td>
<td>5.55</td>
<td>1.33</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Pin = -5 dBm</td>
<td></td>
<td>1.79</td>
<td>-</td>
<td>1.75</td>
<td>0.52</td>
<td>1.55</td>
<td>0.65</td>
</tr>
<tr>
<td>Pin = 0 dBm</td>
<td></td>
<td>0.97</td>
<td>-</td>
<td>0.83</td>
<td>0.26</td>
<td>0.90</td>
<td>0.27</td>
</tr>
<tr>
<td><strong>Area (mm&lt;sup&gt;2&lt;/sup&gt;)</strong></td>
<td></td>
<td>0.22 × 0.27#</td>
<td>0.7 × 0.7</td>
<td>0.5 × 0.43#</td>
<td>0.83 × 0.54</td>
<td>0.36 × 0.64#</td>
<td>0.33 × 0.08#</td>
</tr>
</tbody>
</table>

**Process Technology**

- CMOS in 0.18 µm SiGe BiCMOS, 90 nm CMOS
- 0.18 µm CMOS
- 0.18 µm CMOS
- 0.18 µm CMOS
- 0.18 µm CMOS

**FOM** = \( \left( \frac{\text{Locking Range in %}}{P_{\text{in}} \cdot P_{\text{DC}}} \right) \left( \frac{P_{\text{out}}}{P_{\text{DC}}} \right) \), # - Core area
Conclusion

- The high frequency ILFD divider and the design challenges is discussed.

- High frequency ILFD based on coupled dual LC tanks together with two differential injection transistor pairs to increase the locking range while maintaining a high quality factor is presented.

- The proposed technique is analyzed theoretically and verified experimentally with an ILFD operating at 24 GHz achieving a wide locking range at low injected power levels and higher power efficiency.

- With a compact silicon area and fully differential design, the ILFD can be readily integrated with low power VCOs.
References


Thank You

Q & A
1- Multi-Coupled LC Tanks

Primary LC Tank

Secondary LC Tanks

$K_{i,j}$ is the magnetic coupling among the LCT $i$ and $j$ ($-1 < M_{i,j} < 1$)
2 - Analysis of Multi-Coupled LC Tanks

Dual-Coupled LC tanks

\[
Z_{in,DCLC} = R_{s,DCLC} + j\omega L_{s,DCLC}
\]

\[
Z_{in,DCLC} = R_p + j\omega L_p + \frac{\omega^2 M^2}{R_s + j\omega L_s + (j\omega C_s)^{-1}}
\]

\[
R_{s,DCLC} = R_p + \frac{\omega^2 M^2 R_s}{\omega L_s - (\omega C_s)^{-1}}
\]

\[
L_{s,DCLC} = L_p + \frac{\omega^2 M^2 C_s}{1 - \omega^2 L_s C_s}
\]

\[
Q = \frac{\omega_o L_{s,DCLC}}{R_{s,DCLC}}
\]