Ultra-Low Power Delta Sampling SAR ADC for Sensing Applications

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Outline of Presentation

- Introduction
- Proposed Delta Sampling SAR ADC
- Simulation Results
- Conclusion
Introduction

- ADC requirements in wireless healthcare system:
  - Low Power; Moderate Resolution; Low Sampling Rate
Introduction

ADC Specifications:

- **Accuracy:** 8 bits.
- **Sampling rate:** 100 kS/s.
- **Power:** Sub-µW.

Area of highest energy efficiency.
ECG signal varies slowly except for the QRS complex region.

4 MSBs remain the same during several consecutive samples.
Neural signal varies slowly except for spike periods.

4 MSBs remain the same during several consecutive samples.
Conventional SAR ADC

- Conventional SAR ADC: Binary search from MSB to LSB.
- Not energy-efficient for ECG and neural signal.
Proposed Delta Sampling SAR ADC

Reducing binary search range to achieve low power.
Conventional 2-Stage Dynamic Comparator

Problem: Not applicable for full input common-mode range
Proposed 2-Stage Dynamic Comparator

- **Solution**: Input stage is a combination of NMOS and PMOS.
- If common-mode voltage is high, $I_{n1}$ and $I_{n2}$ will dominate the sum currents $I_{dp}$ and $I_{dn}$.
- If common-mode voltage is low, $I_{p3}$ and $I_{p4}$ will dominate the sum currents $I_{dp}$ and $I_{dn}$. 
Layout of Proposed SAR ADC

- Design in 0.18μm CMOS process.
- 8-bit SAR ADC size: 250μm*470μm.
Simulation Results

ADC performance @ VDD = 1V & fs = 100 kS/s

- SNDR: 46.1 dB
- ENOB: 7.4 bits
- DNL: ±1.3 LSB
- INL: ±1.7 LSB
## Simulation Results

Power consumption for converting neural signal

@ VDD = 1V & fs = 20 kS/s

<table>
<thead>
<tr>
<th>Input Signal</th>
<th>Neural Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V)</td>
<td>1</td>
</tr>
<tr>
<td>Sampling Rate (kS/s)</td>
<td>20</td>
</tr>
<tr>
<td>ENOB (bit)</td>
<td>7.4</td>
</tr>
</tbody>
</table>

### Power (nW)

<table>
<thead>
<tr>
<th>Power (nW)</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor Arrays</td>
<td>25.4</td>
</tr>
<tr>
<td>Comparator</td>
<td>55.1</td>
</tr>
<tr>
<td>Digital Circuits</td>
<td>131.4</td>
</tr>
</tbody>
</table>

- Conventional SAR ADC consumes 1280nW.
- This proposed delta sampling SAR ADC can save 83% power.
Conclusion

- Conventional SAR ADC is not energy-efficient to convert slow varying signals, such as ECG & Neural Signal;
- Delta sampling SAR ADC reduces binary search range to save power;
- The input common-mode range of dynamic comparator is widened by using a combination of NMOS and PMOS in the input stage.
THANK YOU